REMARKS

The application contains claims 1, 3-7, 9-12 and 17-20. In view of the foregoing amendments and following remarks, Applicants respectfully request allowance of the application.

SUBSTANCE OF THE INTERVIEW

At the outset, Applicants thank Examiner Huisman for the courtesy of the November 19, 2003 interview with the undersigned. At the interview, the undersigned presented a general introduction of the subject matter of the invention and a comparison to the prior art. The Examiner encouraged the undersigned to present a formal amendment, which is now done.

CLAIM/SPECIFICATION OBJECTIONS

The foregoing amendments overcome the specification objections and claim objections noted in paragraphs 3-5 of the office action.

With respect to the objections to "the one pipestage" (para. 4, 5), Applicants suggest no amendment is necessary. For both the first and second pipestages, claim 17 singles out one pipestage therein as being in communication with the return stack buffer. The dependent claims clearly refer to this singled-out pipestage. The Examiner is authorized to add the phrase –in communication with the return stack buffer— by Examiner's amendment if deemed absolutely necessary, but Applicants disfavor this approach because it reduces the readability of the claims and they are sufficiently clear as they stand.

PRIOR ART REJECTIONS

All pending claims stand rejected based on prior art. Applicants respectfully request withdrawal of these outstanding rejections because the prior art does not teach or suggest all elements of the pending claims.

Claims 1 and 3 are allowable over the cited art.

Consider claim 1, which stands rejected as obvious over Hennessy and Hoyt. It recites:

> determining, with reference to other instructions read previously from the instruction pipestage, whether a return address associated with the return instruction can be written immediately to a next instruction pipestage and,
>
> stalling processing of the return instruction until the return address associated with the return instruction can be written to the next instruction pipestage.

The cited art does not teach or suggest this subject matter. The cited portion of Hennessy (p. 154, FIG. 3.13) deals with data read from a cache. Any teaching of this portion of the cited art is of minimal relevance to claim 1, where the focus is on a ***return address*** associated with a return instruction. As noted by both Hennessy and Applicants' disclosure, call and return instructions address a return stack buffer – a system that is separate from the cache described on p. 154. Applicants are unaware that Hennessy has any teaching or suggestion to stall any part of his system when processing call or return instructions.

Hoyt also fails to teach or suggest the claimed subject matter. While the Examiner argues that Hoyt teaches stalling in the context of return instructions, Hoyt's disclosure actually is devoted to prediction of return addresses. Prediction generally is performed to generate data to avoid the necessity of stalls. See, Hoyt, Cols. 1:37-62, 2:32-36 (desirable to predict return addresses so the processor does not need to stall).

Claim 1 recites that a method determines whether the return address is immediately available and stalls processing of the return instruction when it is not. Neither Hoyt nor Hennessy disclose determining whether a return instruction is immediately present in a pipestage. Accordingly, claims 1 and 3 are allowable.

Claims 4-6 are allowable over the cited art.

Claim 4 stands rejected as anticipated by Hennessy. Claim 4 has been amended to recite:

> determining, with reference to other instructions read previously from the instruction pipestage, whether immediate processing of the call instruction would exceed a predetermined access rate of the instruction pipe to a return-stack buffer and,
>
> stalling processing of the call new instruction until sufficient time has expired to synchronize processing of the call instruction with the predetermined access rate.

Hennessy does not teach or suggest this subject matter. The various hazards described by Hennessy on p. 154 do not apply to call instructions and do not involve return stack buffers. Accordingly, claims 4-6 define over this art.

Claims 7 and 9 are allowable over the cited art.

Claims 7 and 9 stand rejected as obvious over Hennessy and Hoyt. Applicants respectfully request reconsideration because the cited art does not teach or suggest all elements of the claims. Claim 7, for example, recites:

> storing a return address associated with the call instruction both locally and in a shared resource.

None of the cited art teaches or suggests this subject matter in the context of processing a call instruction. Neither reference teaches or suggests storing a return address in two places, a local place and in a shared resource. Accordingly, claims 7 and 9 define over the art.

Applicants respectfully suggest that the office action's analysis with respect to prediction of return addresses does not apply to processing of call instructions. Prediction occurs to speed processing of a return instruction. There is no prediction to be performed pursuant to a call – the call causes instruction execution to move from a present instruction to a new instruction. When performing a call, the return address is known exactly; it is the very next instruction following the present instruction. No system, to the undersigned's knowledge, ever predicts return instructions in connection with a call instruction. Applicant also is unaware of any system that stores a return instruction in two places during performance of a call. Typically, return addresses are stored only in a return stack buffer.

Claims 10-12 are allowable over the prior art.

Claim 10-12 stand rejected as anticipated by Hennessy, p. 154 and FIG. 3.13. Claim 10 now recites:

> determining, with reference to other instructions read previously from the instruction pipestage, whether a return address is available to the instruction pipe prior to expiration of the round-trip communication latency period with the return-stack buffer

Claim 10 now expressly refers to a round-trip communication latency with a return-stack buffer. Hennessy's discussion in p. 154 deals only with conflicts that occur when accessing a common memory. Accordingly, claim 10 defines over this art.

New claims

New claims 21-26 are presented for examination. Claims 21-22 depend from claim 1 and recite further operation of the claimed method. Independent claim 23 recites passing a return address from immediate local storage or from a return stack buffer. Independent claim 25 recites a pair of local storage devices, one receiving a return instruction from within the instruction pipe and the other receiving an instruction from a return stack buffer. All newly proposed claims are believed to define over the cited art.

All claims stand in condition for allowance. Applicants respectfully request allowance of the application.

Respectfully submitted,

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